256Kx32 SRAM MODULE *ADVANCED**

FEATURES

- Access Times**
  - BiCMOS: 10ns
  - CMOS: 12, 15, 20, 35ns
- Packaging
  - Module is manufactured with eight 256Kx4 SRAM memory devices on laminate substrate
  - 64 pin SIMM, JEDEC Standard Pinout
  - 64 pin ZIP
  - 64 pin ZIP, Low Profile**
- Organized as 256Kx32
- Commercial Temperature Range
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

** *Low Profile ZIP only available in 20 and 35ns access time.*

FIG. 1 PIN CONFIGURATION FOR WPS256K32-XXC

TOP VIEW

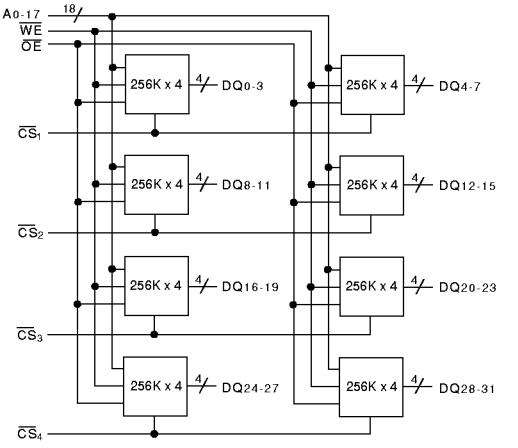
Vss	1	$\overline{CS}4$	33
PD0	2	$\overline{CS}3$	34
PD1	3	A17	35
DQ0	4	A16	36
DQ8	5	$\overline{OE}$	37
DQ1	6	Vss	38
DQ9	7	DQ24	39
DQ2	8	DQ16	40
DQ10	9	DQ25	41
DQ3	10	DQ17	42
DQ11	11	DQ26	43
Vcc	12	DQ18	44
A0	13	DQ27	45
A7	14	DQ19	46
A1	15	A3	47
A8	16	A10	48
A2	17	A4	49
A9	18	A11	50
DQ12	19	A5	51
DQ4	20	A12	52
DQ13	21	Vcc	53
DQ5	22	A13	54
DQ14	23	A6	55
DQ6	24	DQ20	56
DQ15	25	DQ28	57
DQ7	26	DQ21	58
Vss	27	DQ29	59
$\overline{WE}$	28	DQ22	60
A15	29	DQ30	61
A14	30	DQ23	62
$\overline{CS}2$	31	DQ31	63
$\overline{CS}1$	32	Vss	64

PD0	—	Vss
PD1	—	Vss

PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
PD0-1	Presence Detect
Vcc	Power Supply
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_{STG}	-55	+125	°C
Signal Voltage Relative to GND	V_G	-0.5	7.0	V
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp	T_A	0	+70	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	60	pF
$\overline{WE}$	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	60	pF
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	60	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	10		12, 15, 20, 35		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vss to Vcc		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Vss to Vcc		10		10	µA
Operating Supply Current x 32 Mode	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		1040		1040	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		180		75	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	-10		-12		-15		-20		-35		Units
Read Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Read Cycle Time	t_{RC}	10		12		15		20		35		ns
Address Access Time	t_{AA}		10		12		15		20		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		10		12		15		20		35	ns
Output Enable to Output Valid	t_{OE}		7		8		9		9		12	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		8		9		9		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		8		9		9		12	ns

1. This parameter is guaranteed by design but not tested.

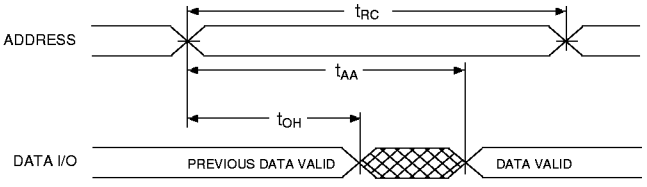
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

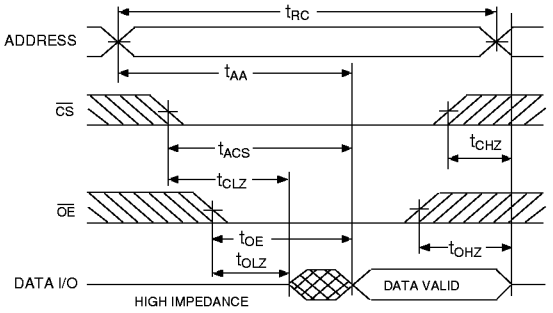
Parameter	Symbol	-10		-12		-15		-20		-35		Units
Write Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	t_{WC}	10		12		15		20		35		ns
Chip Select to End of Write	t_{CW}	8		9		11		13		15		ns
Address Valid to End of Write	t_{AW}	8		9		11		13		15		ns
Data Valid to End of Write	t_{DW}	6		7		8		10		12		ns
Write Pulse Width	t_{WP}	8		9		11		13		15		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	2		2		2		2		2		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]	0	7	0	8	0	9	0	9	0	12	ns
Data Hold Time	t_{DH}	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
TIMING WAVEFORM - READ CYCLE

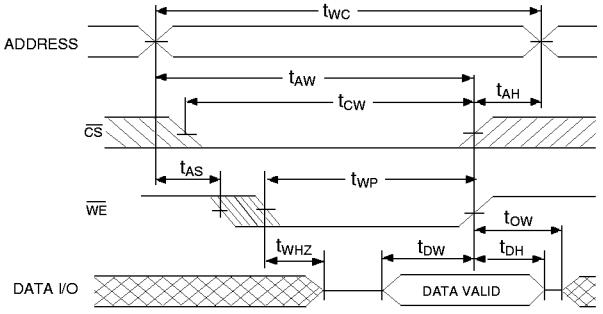


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



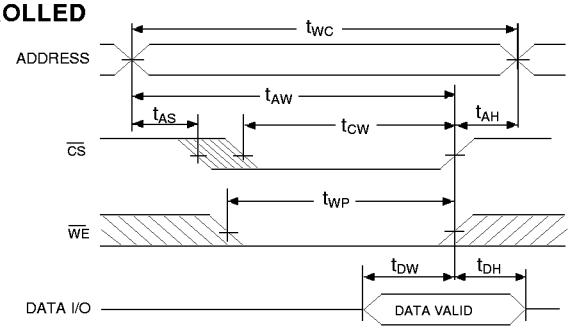
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED



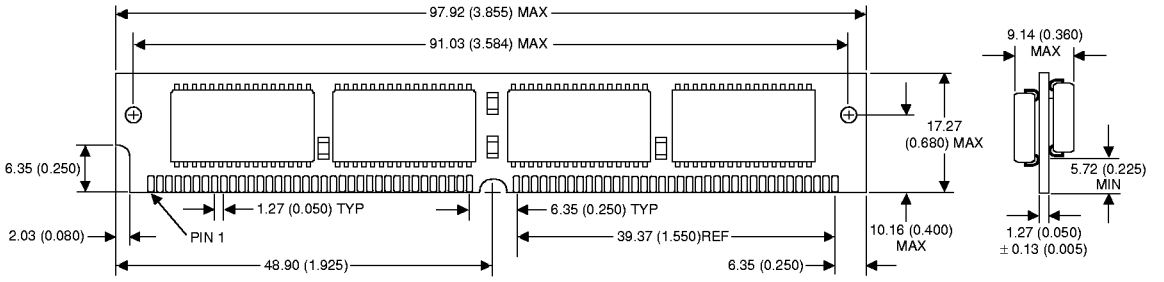
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED



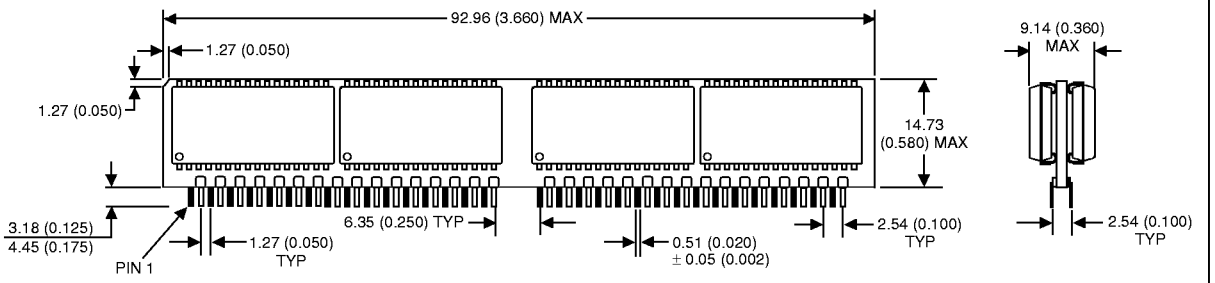
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

FIG. 5
PACKAGE DRAWING 64-PIN SIMM (NS)



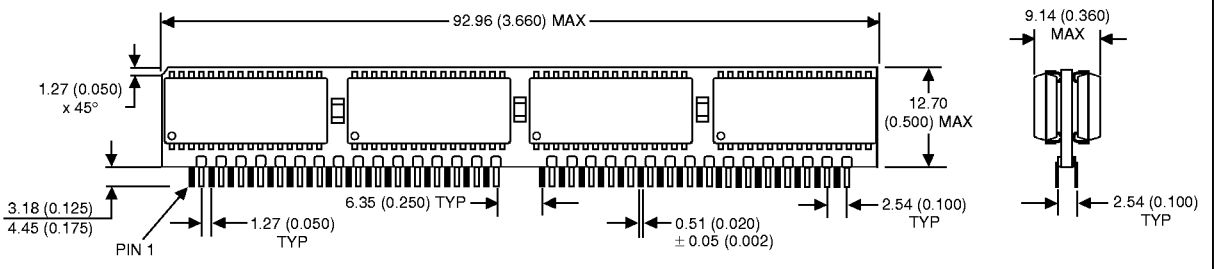
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 6
PACKAGE DRAWING 64-PIN ZIP (TZ)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 7
PACKAGE DRAWING 64-PIN ZIP, LOW PROFILE (NZ)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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